# Department Of Computer Science and Engineering <br> Kathmandu University <br> Dhulikhel, Kavre 

## Subject: Electronics Engineering I

Course: EEEG 202
Level: B.E./B.Sc/B. Tech. $2^{\text {nd }}$ Year/ $1^{\text {st }}$ Semester Credit Hours: 3

Objective: To introduce students to the fundamental concepts of digital logic

## Syllabus:

Introduction to Digital Systems: Why digital?; Analogue versus digital
Number Systems and Codes: Binary, octal and hexadecimal number systems; Conversion from one number system to another; Representation of negative numbers by signed magnitude representation, radix-complement representation ( 2 's complement and 10 's complement), diminished radix-complement representation (1's complement and 9's complement); Addition and subtraction of negative numbers; Binary, hexadecimal and octal numbers; 1's and 9's complements, and 2's and 10's complements; Binary multiplication and division; Problem of overflow in arithmetic operation; Weighted and unweighted binary codes, excess-3 and Gray codes; Error detecting codes (parity); Alphanumeric, ASCII and EBCDIC codes

Boolean Algebra and Logic Gates: Introduction; Postulates of Boolean algebra, associativity, inverse, closure, commutativity, and distributivity; Basic theorems and properties of Boolean algebra and duality; Boolean variables and constants, algebraic manipulation, maxterms, minterms and conversion between them; Two variable Boolean algebra and switching algebra; Digital logic gates; IC digital logic families; An introduction to TTL, ECL, MOS, CMOS, I2L.

Simplification of Boolean Functions: Map method: 2,3, and 4 variable maps; Product of sums simplification; Implementation of digital functions using universal gates (NAND and NOR); Don't care conditions; The tabulation method - detection and selection of prime implicants

Combinational Logic: Introduction; Active level designation for logic gate pins; Useful digital circuits implemented through combinational logic - half and full adders, half and full subtractors, BCD to excess 3 code converter, binary parallel adder, look ahead carry generator, BCD adders, magnitude comparator, decoders, encoders and priority encoders, multiplexers and demultiplexers; Combinational circuit analysis procedures and combination circuit realisation using universal gates; Block diagram transformation of combinational logic circuits implemented by one type of gate to another; Use of multiplexers and decoders for combinational logic design; Introduction to ROM and PLA and their use in combination logic circuits.

Sequential Logic circuits: Introduction; Distinction between combinational and sequential circuits; Bistables, master-slave and edge triggered; Design of clocked bistables; Conversion from one type to another; Analysis of sequential circuit using state diagrams; Bistable excitation
tables; Design of sequential circuit using state reduction method (e.g. single mode counter, modulo-n counter)

Registers, Counters and Memories: Introduction; Registers as basic memory blocks; Registers with parallel load, shift registers, bidirectional shift registers with parallel load; Ripple counters, binary and BCD ripple counters, binary counters, binary up/down counters, BCD, Johnson and ring counters; Introduction to memory units, memory address registers and memory buffer registers.

## References:

1. M M Mano, Digital Design, Prentice Hall India
